REMARKS

Claims 1-6, 8-13 and 15-20 are in the application. Claims 7 and 14 have been cancelled previously.

By this amendment, claims 1, 12 and 18 have been amended to more particularly point out the subject matter of applicant's invention. FIG. 1 and paragraph [0015] support the changes to these claims.

Response to 35 U.S.C. §103 Rejections

Claims 1-6, 8-13, and 15-20 were rejected under 35 U.S.C. §103 as being obvious over Blanchard et al., USP 6,750,104 (hereafter "Blanchard A") in view of Blanchard, USP 4,914,058 (hereafter "Blanchard B"). This rejection is respectfully traversed in view the amendments made herein and the remarks presented hereinafter.

Claim 1 now calls for a method of making a semiconductor vertical trench gate junction FET device including the steps of providing a body of semiconductor material comprising a first conductivity type, wherein the body of semiconductor material has an upper surface and a lower surface opposing the upper surface, wherein the lower surface provides a drain contact. The method also calls for forming a first trench in the body of semiconductor material and extending from the upper surface, wherein the first trench has a first width, a first depth from the upper surface, first sidewalls, and a first bottom surface. The method additionally calls for forming a second trench within the first trench, wherein the second trench has a second width, a second depth from the first surface, second

sidewalls and a second bottom surface. The method further calls for forming a first source region in the body of semiconductor material extending from the upper surface and spaced apart from the first trench by a portion of the body of semiconductor material. The method still further calls for introducing a dopant of a second conductivity type into at least a portion of the second sidewalls and the second bottom surface to form a doped trench gate region, wherein the doped trench gate region extends into the body of semiconductor material for controlling conduction in the device. Moreover, the method calls for forming a first passivation layer over the doped trench gate region, and forming a second passivation layer over the first passivation layer thereby filling at least the second trench.

Applicant respectfully submits that the Blanchard A and B references fail to make claim 1 obvious for at least the following reasons.

1. Neither reference, either singularly or in combination, shows or suggests a vertical trench gate junction FET device where the gate region is formed by introducing dopant through the sidewalls and bottom surface of a second trench region, and where the gate region extends into a body of semiconductor material.

In Blanchard A, the device shown is a planar gated device as is evident in FIG. 5 and further described in Col. 5, lines 33-37. In this device, Blanchard A's gate region 18 is separated from the body of semiconductor material, and does not within the body of semiconductor material, nor is it formed by introducing dopant through the sidewalls and bottom surface of a second trench as is called for in claim

1. Additionally, portion 520 of Blanchard A's device is not a gate region at all, but is a p-type column "voltage sustaining region", which is used to control the breakdown voltage of Blanchard A's device (see Col. 5, lines 9-52) not for controlling conduction in the device. Applicant respectfully submits that region 520 clearly is not a gate region, nor is suggestive in any way of one. In Blanchard B's device, the gate region 34 is not formed by introducing dopant through sidewall and bottom surfaces of the second trench nor does it extend into the body of semiconductor material as is called for in claim 1. Instead, region 34 is formed separated from the body of semiconductor material by a dielectric layer 32 as is evident in FIG. 4i of Blanchard B.

2. The combination of Blanchard '104 and '058 does not show or suggest applicant's method of forming a trench gate region JFET device.

Applicant respectfully submits that at best, the combination of Blanchard A and Blanchard B would result in a trench gated MOSFET where the Blanchard B gate region 34 is separated from the body of semiconductor material by a dielectric layer 32 together with a Blanchard A column "voltage sustaining region" 520 formed underneath Blanchard A's P body regions 20a and 20b. However, this still does not show or suggest applicant's claimed invention where the doped gate region is formed by introducing dopant of a second conductivity type into the body of semiconductor material through at least portions of the sidewalls and bottom surface of the second trench and extending within the body of semiconductor material as required by claim 1.

3. The combination of Blanchard A and B would render Blanchard's MOSFET device inoperable.

As stated above, Blanchard's A device shows a column "voltage sustaining region", which clearly is not a gate region. Further, Blanchard A's gate region 18 is planar, and is not formed by introducing dopant into the body of semiconductor material as required by claim 1. Applicant further submits that there is no motivation to take region 512 from Blanchard A and to combine it with Blanchard B to place region 512 in the vicinity of Blanchard B's gate region because to do so would destroy the MOSFET action of Blanchard B's device. Specifically, p-type region 512 would counter-dope Blanchard's n-type drain region 11 and change the channel characteristics and performance of the device. It is well accepted that when the functionality of a device would be destroyed or detrimentally impacted by a combination, there is strong evidence of non-obviousness as is the case here.

4. Neither reference teaches or suggests forming a second passivation layer over a first passivation thereby filling at least the second trench.

Blanchard A only shows a single trench structure, which is not a trench within a trench, and further only shows a single passivation layer within the single trench. In Blanchard B, the second trench is not filled with a second passivation layer, but instead is filled with a conductive layer - doped polysilicon 34 (see Blanchard B, Col. 5, lines 37 to 68). Thus, neither reference shows or suggests this additional element.

5. Claim 1 calls for a method of forming a trench gate junction FET device.

In Blanchard A and B, methods of forming MOSFET devices are shown, not methods for forming a JFET device as is called for in claim 1. Further, even though Blanchard A suggests a JFET device at Col. 6 line 11, Blanchard's "voltage sustaining region" 520 is irrelevant to applicant's claimed invention because Blanchard's "voltage sustaining region" has absolutely nothing to do with a gate region or controlling conduction within the device.

For at least the above five (5) reasons, applicant respectfully submits that claim 1 is allowable over the cited Blanchard references.

Claims 2-6, and 8-11 depend from claim 1 and are believed allowable for at least the same reasons as claim 1.

Claim 12 calls for a process for making a compound semiconductor vertical trench gate junction FET device comprising the steps of forming a first groove in a compound semiconductor layer of a first conductivity type, wherein the first groove has first sidewalls and a first lower surface, and wherein the first groove extends from a first surface of the compound semiconductor layer. The process also calls for forming a second groove within the first groove, wherein the second groove has second sidewalls and a second lower surface. In addition, the process includes doping the second lower surface and at least a portion of the second sidewalls with a second conductivity type dopant to form a doped trench gate region in the compound semiconductor layer, and forming a first source region of the first conductivity type in the compound semiconductor

layer adjacent to the first groove. Additionally, the process includes forming a source contact to the first source region, and filling the second groove and at least a portion of the first groove with a passivation layer. Further, the process calls for forming a gate contact coupled to the doped trench gate region, and forming a drain contact on a second surface of the compound semiconductor layer.

Applicant respectfully submits that the Blanchard A and B references fail to make claim 12 obvious for at least the following reasons.

1. Neither reference, either singularly or in combination, shows or suggests a vertical trench gate junction FET device where the doped trench gate region is formed in a compound semiconductor layer by doping the second lower surface and at least a portion of the second sidewalls with a second conductivity type dpdant.

In Blanchard A, the device shown is a planar gated device as is evident in FIG. 5 and further described in Col. 5, lines 33-37. In this device, Blanchard A's gate region 18 is separated from the body of semiconductor material, and is not formed by doping portions of the sidewalls and lower surface of a second trench as is called for in claim 12. Additionally, portion 520 of Blanchard A's device is not a gate region at all, but is a p-type column "voltage sustaining region", which is used to control the breakdown voltage of Blanchard's device (see Col. 5, lines 9-52) not for controlling conduction in the device. Applicant respectfully submits that region 520 clearly is not a gate region, nor is suggestive in any way of one.

In Blanchard B's device, the gate region 34 is not formed within a compound semiconductor layer as is called for in claim 12, but instead, is formed separated from the body of semiconductor material by a dielectric layer 32 as is evident in FIG. 4i in Blanchard B.

2. Claim 12 calls for a process for making a compound semiconductor vertical trench gate junction FET device.

In Blanchard A and B, methods of forming silicon MOSFET devices are shown, but not methods of forming a compound semiconductor JFET device as is called for in claim 12. Further, even though Blanchard A suggests a JFET device at Col. 6 line 11, Blanchard's "voltage sustaining region" is irrelevant to applicant's claimed invention because it has absolutely nothing to do with forming a gate region that controls conduction in the device.

3. The combination of Blanchard '104 and '058 does not show or suggest applicant's process of forming a trench gate region JFET device.

Applicant respectfully submits that at best, the combination of Blanchard A and Blanchard B would result in a trench gated MOSFET where the Blanchard B gate region 34 is separated from the body of semiconductor material by a dielectric layer 32 together with a Blanchard's A column "voltage sustaining region" 520 formed underneath P body regions 20a and 20b of Blanchard B. However, this still does not show or suggest applicant's claimed invention where the doped gate region is formed by doping portions of the sidewall and lower surfaces of a second groove, and where the doped gate region is physically within the compound

semiconductor material and not separated therefrom by a dielectric layer as is the case in both Blanchard references.

4. The combination of Blanchard A and B would render Blanchard's MOSFET device inoperable.

As stated above, Blanchard's A device shows a column "voltage sustaining region", which clearly is not a gate region. Further, Blanchard A's gate region 18 is planar, and is not within the compound semiconductor material as required by claim 12. Applicant further submits that there is no motivation to take region 512 from Blanchard A and to combine it with Blanchard B to place region 512 in the vicinity of Blanchard B's gate region because to do so would destroy the MOSFET action of Blanchard B's device. Specifically, p-type region 512 would counter-dope Blanchard's n-type drain region 11, and change the channel characteristics and performance of the device. It is well accepted that when the functionality of a device would be destroyed or detrimentally impacted by a combination, there is strong evidence of non-obviousness as is the case here.

5. Neither Blanchard reference shows or suggests a step of filling the second groove and at least a portion of the first groove with a passivation layer.

Blanchard A only shows a single trench structure, which is not a trench within a trench, and further only shows a single passivation layer within the single trench. In Blanchard B, the second trench is not filled with a second passivation layer, but instead is filled with a conductive

layer - doped polysilicon 34 (see Blanchard B, Col. 5, lines 37 to 68).

For at least the above five (5) reasons, applicant respectfully submits that claim 12 is allowable over the cited Blanchard references.

Claims 13 & 15-17 depend from claim 12 and are believed allowable for at least the same reasons as claim 12.

Claim 18 calls for a method for forming a compound semiconductor trench gate junction FET device comprising the steps of providing a body of compound semiconductor material including a support wafer of a first conductivity type and a first dopant level and an epitaxial layer formed over the support wafer, wherein the epitaxial layer is of the first conductivity type and has a second dopant level lower than the first dopant level. The method also calls for forming a plurality of spaced apart first doped regions of the first conductivity type in the epitaxial layer, and forming a plurality of first trenches in the epitaxial layer, wherein each first trench is between a pair of first doped regions. Additionally, the method calls for forming a plurality of second trenches in the epitaxial layer, wherein one second trench is within one first trench, and doping at least portions of sidewall surfaces and lower surfaces of each second trench to form a plurality of doped trench gate regions, wherein the plurality of doped gate regions extend into the body of compound semiconductor material. Moreover, the method calls for filling the plurality of second trenches and at least a portion of the plurality of first trenches with a passivation material. In addition, the method calls for coupling the plurality of spaced apart first doped regions with a first contact layer, and coupling

the plurality of doped trench gate regions to a gate connecting region formed in the body of compound semiconductor material. Further, the method calls for forming a drain contact on a second surface of the support wafer.

Applicant respectfully submits that the Blanchard A and B references fail to make claim 12 obvious for at least the following reasons.

1. Neither reference, either singularly or in combination, shows or suggests a method of forming a compound semiconductor trench gate junction FET device where the gate regions are formed by doping at least portions of sidewall surfaces and lower surfaces of each second trench, wherein the plurality of doped gate regions extend into the body of compound semiconductor material.

In Blanchard A, the device shown is a planar gated device as is evident in FIG. 5 and further described in Col. 5, lines 33-37. In this device, Blanchard A's gate region 18 is separated from the body of semiconductor material, and is not formed by doping the body of semiconductor material so that the gate region extends into a compound semiconductor layer as is further called for in claim 1. Additionally, portion 520 of Blanchard A's device is not a gate region at all, but is a p-type column "voltage sustaining region", which is used to control the breakdown voltage of Blanchard's device (see Col. 5, lines 9-52) not for controlling conduction in the device. Applicant respectfully submits that region 520 clearly is not a gate region, nor is suggestive in any way of one. In Blanchard B's device, the gate region 34 is not formed within the body of semiconductor material as is called for in claim 18, but instead, if formed separated from the body of semiconductor

material by a dielectric layer 32 as is evident in FIG. 4i of Blanchard B.

2. Claim 12 calls for a process for making a compound semiconductor vertical trench gate junction FET device.

In Blanchard A and B, methods of forming silicon MOSFET devices are shown, but not methods of forming a compound semiconductor trench gate JFET device as is called for in claim 18. Further, even though Blanchard A suggests a JFET device at Col. 6 line 11, Blanchard's "voltage sustaining region" is irrelevant to applicant's claimed invention because it has absolutely nothing to do with a gate region.

3. The combination of Blanchard '104 and '058 does not show or suggest applicant's process of forming a trench gate region JFET device.

Applicant respectfully submits that at best, the combination of Blanchard A and Blanchard B would result in a trench gated MOSFET where the Blanchard B gate region 34 is separated from the body of semiconductor material by a dielectric layer 32 together with a Blanchard A column "voltage sustaining region" 520 formed underneath P body regions 20a and 20b of Blanchard B. However, this still does not show or suggest applicant's claimed invention where the doped gate regions are formed by doping at least portions of sidewall and lower surfaces of each second trench so that the doped gate regions are physically within the compound semiconductor material.

4. The combination of Blanchard A and B would render Blanchard's MOSFET device inoperable.

As stated above, Blanchard's A device shows a column "voltage sustaining region", which clearly is not a gate region. Further, Blanchard A's gate region 18 is planar, and is not within the compound semiconductor material as required by claim 12. Applicant further submits that there is no motivation to take region 512 from Blanchard A and to combine it with Blanchard B to place region 512 in the vicinity of Blanchard B's gate region because to do so would destroy the MOSFET action of Blanchard B's device. Specifically, p-type region 512 would counter-dope Blanchard's n-type drain region 11, and change the channel characteristics and performance of the device. It is well accepted that when the functionality of a device would be destroyed or detrimentally impacted by a combination, there is strong evidence of non-obviousness as is the case here.

5. Neither Blanchard reference shows or suggests a step of filling the plurality of second trenches and at least a portion of the plurality of first trenches with a passivation material.

Blanchard A only shows a single trench structure, which is not a trench within a trench, and further only shows a single passivation layer within the single trench. In Blanchard B, the second trench is not filled with a second passivation layer, but instead is filled with a conductive layer - doped polysilicon 34 (see Blanchard B, Col. 5, lines 37 to 68).

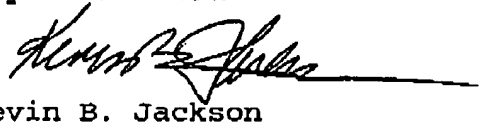
For at least the above five (5) reasons, applicant respectfully submits that claim 18 is allowable over the cited Blanchard references.

Claims 19 and 20 depend from claim 18 and are believed allowable for at least the same reasons as claim 18.

In view of all of the above, it is believed that the claims are allowable, and the case is now in condition for allowance, which action is earnestly solicited.

Respectfully submitted,

Peyman Hadizad



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